The UNIVERSITY *of* NORTH CAROLINA *at* CHAPEL HILL

Comp 411 Computer Organization
Spring 2014

Problem Set #5
Issued Wednesday, 3/26/14; Due Tuesday, 4/1/14
(hand in your work at start of class)

Note: You may use additional sheets of paper, but please enter your answers in the space provided in this document.

Problem 1. "Bits of Floating-Point" (28 points)

Represent the following in *single-precision* IEEE floating point. Give your answers in *hexadecimal.* Enter the answers in the table.

a) –246.0
b) $(2^{10} - 1)$

Decimal	***S field***	***E field (binary)***	***F field (binary)***	***Complete Number (Hex)***
–246.0	1	10000110	1110 1100 0000 0000 0000 000	0xc3760000
$(2^{10} - 1)$	0	10001000	1111 1111 1000 0000 0000 000	0x44FC0000

Convert the following single-precision floating-point number (given in hexadecimal) to decimal, and enter the answer in the table below:

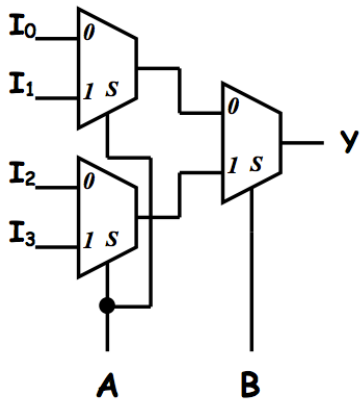
c) 0xa9c30000

After you determine the *S, E,* and *F* fields, compute the decimal value using a calculator.

Hex	***S field***	***E field (binary)***	***Significand (binary)***	***Decimal (using calculator)***
A9C30000	1	01010011	100 0011 0000 0000 0000 0000	-8.659739 x 10^-14

Problem 2. Multiplexers (36 points)

Suppose you wanted to implement a Boolean function *Y* of two inputs *A* and *B* using multiplexers, as shown in the figure.

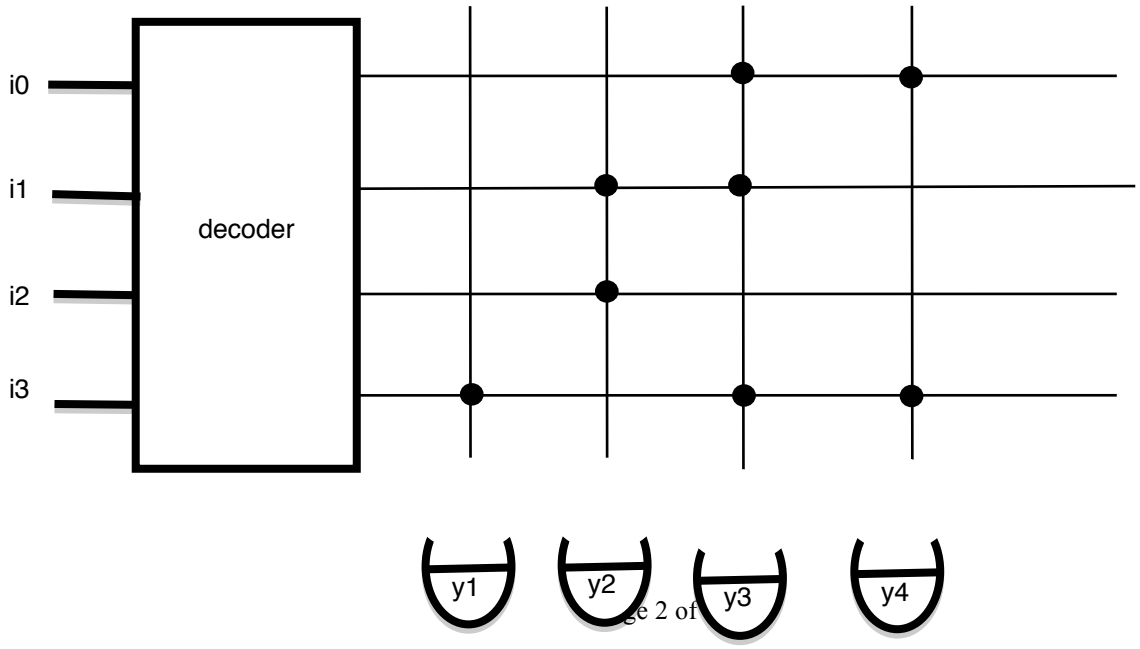


In the table below, enter the binary values for I_0, I_1, I_2, and I_3 that implement the following functions on the two inputs *A* and *B:*

a) Y_1 = AND(A,B)
b) Y_2 = XOR(A,B)
c) Y_3 = (A>=B)
d) Y_4 = (A==B)

Function Y =	I_0	I_1	I_2	I_3
AND(A,B)	0	0	0	1
XOR(A,B)	0	1	1	0
A>=B	1	1	0	1
A==B	1	0	0	1

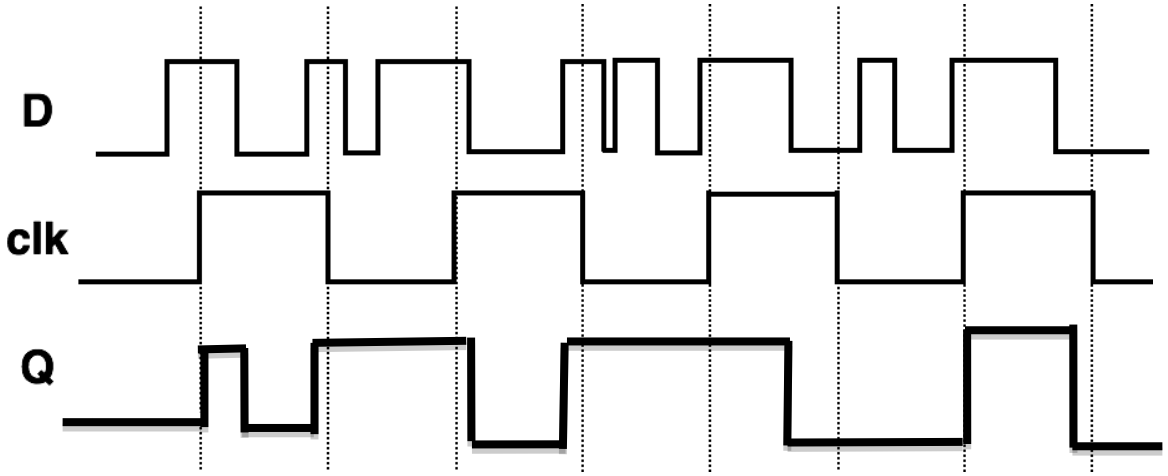
e) For this question, refer to slide 8 in Lecture 13. For the above figure, draw the corresponding decoder and outputs, making sure to clearly indicate which fuses are intact. Indicate a connection with a dark disk at the intersection; if no connection is made, leave the intersection blank.



Problem 3: Latches and Flip-Flops. (36 points)

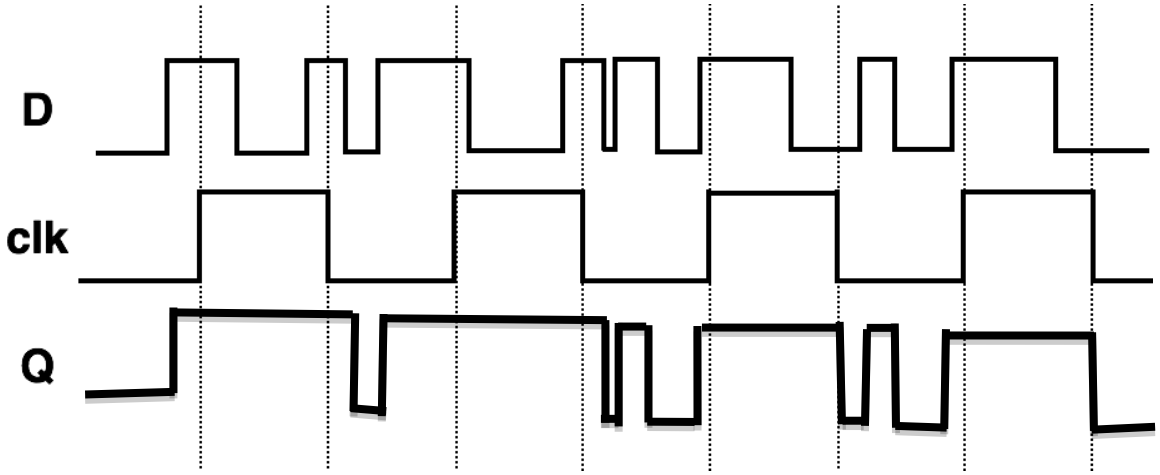
In the questions below, assume propagation delays, setup times and hold times are negligible.

a) The figure below shows the input *D* to a *positive latch*, along with the clock control input, *clk.* Draw the output waveform *Q*.



Positive latch means that the input, D, is pointed to the 1

b) The figure below shows the input *D* to a *negative latch*, along with the clock control input, *clk.* Draw the output waveform *Q*.



Negative latch means that the input, D, is pointed to the 0

Assuming master is closed when clk is high (and master is first)

c) The figure below shows the input *D* to a *flip flop (master-slave latch pair)*, along with the clock control input, *clk.* Draw the output waveform *Q*. *[Note: It is not necessary to draw the internal ("star") waveform.]*